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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,595	08/09/2001	Gregory Francis Pfister	AUS920010495US1	5434

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Duke W. Yee
Carstens, Yee & Cahoon, LLP
P.O. Box 802334
Dallas, TX 75380

EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	4

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,595	PFISTER ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-38 are presented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 10/16/2001 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 24 recite the limitation "the buffer" in last line of both claims. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Gharachorloo et al., US 2002/0007439 A1.

Regarding claims 1,20 and 36, Gharachorloo teaches that a method in a data processing system for managing cached data, the method comprising:

responsive to initiating a read operation on a block of data (Fig.11A, step 1100, col.12, section 0154, lines 2-5), placing an indication (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) on a directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) identifying the data processing system as containing a copy of the data block with a location (state bits 2b in the directory entry 182) in the data processing system in which a flag (state field 186) associated the data block is located (col.12, section 0154); and

responsive to initiating a write operation on the data block (Fig.12A, step 1200, col.13, section 0165, lines 3-5), sending a message (it is taught as send read-exclusive request to the home node, Fig.12A, step 1214 to step 1230) to all other data processing systems identified in the directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) as containing a copy of the data block (Fig.12B, a shared copy of the memory line 184) to reset the flag (Fig.12B and Fig.12C, step 1203-1234) such that the flag indicates that the data in the data block is invalid (Fig.12C, step 1233-1234) without requiring any action by the other data processing systems receiving the message (col.14, section 0169, last 8 lines).

Regarding claims 2 and 21, Gharachorloo teaches that the directory of data blocks is located in at least one of the data processing system and the other data processing systems (col.5, section 0064, first three lines and section 0065, last four lines).

Regarding claims 3 and 22, Gharachorloo teaches that the data block is a page (col.5, section 0064, lines 8-13).

Regarding claims 4 and 23, Gharachorloo teaches that a method in a data processing system for managing a plurality of caches of data, wherein the data processing system includes a plurality of processors (Fig.1 and 2, CPUs 106), the method comprising:

dedicating a processor within the plurality of processors for polling for request messages from other data processing systems (col.12, section 0153, lines 11-12); responsive to initiating a read operation to read data on a data block (Fig.11A, step 1100, col.12, section 0154, lines 2-5), posting an indication (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) on a directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) identifying the read operation by the data processing system (Fig.11A to Fig.11E); and

responsive to initiating a write operation on the data block (Fig.12A, step 1200, col.13, section 0165, lines 3-5), sending a message (it is taught as send read-exclusive request to the home node, Fig.12A, step 1214 to step 1230) to all of the other data processing systems that the data block is invalid (Fig.12C, step 1233-1234) to remove the data block from the directory of data blocks (Fig.12C, step 1235; col.14, section 0167, last seven lines).

Regarding claims 5 and 24, Gharachorloo teaches that further comprising:

obtaining a lock on a data block (it is taught as the state within the directory entry 182);

determining whether a copy of the data block is present within a local cache (Fig.11A step 1102); and

responsive to a copy of the data block being absent from the local cache (Fig.11a step 1102-No), checking a validity of the data block in the buffer (it is taught as checking

the state of the memory line of information, Fig.11B-C, step 1120 to 1122; col.13, section 0157, lines 4-8).

Regarding claims 6 and 25, Gharachorloo teaches that further comprising: providing a lock table (it is taught as directory 180 in Fig.4), wherein the lock table contains data (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) identifying the data processing system and a location of a validity flag (state field 186) in which the validity flag indicates whether the data block is valid.

Regarding claims 7 and 26, Gharachorloo teaches that the data block is a page (col.5, section 0064, lines 8-13).

Regarding claims 8 and 27, Gharachorloo teaches that the message initiates an invalidation of the data block (Fig.12C, step 1233-1234).

Regarding claims 9 and 28, Gharachorloo teaches that a method in a data processing system for managing data in a distributed buffer system, the method comprising:

identifying an operation to access the data (Fig. 11A, identifying a read operation for a memory line of information 184);

determining whether a copy of the data is present locally within the data processing system (Fig.11A, step 1102; col.12, section 0154, lines 5-6);

responsive to the copy of the data being present locally within the data processing system (Fgi.11A, step 1104), checking an indicator (check directory 180) for the data to determine whether the copy of the data is valid (check directory 180 to determine if the state of the memory line of information is exclusive which indicating a node has an exclusive copy of the corresponding memory line of information); and

responsive to the data being valid, accessing the copy of the data (Fig.11b, step 1158).

Regarding claims 10 and 29, Gharachorloo teaches that further comprising:

responsive to an absence of a copy of the data being present locally within the data processing system (Fig.11a step 1102-No), copying the data into the data processing system (Fig.11D, step 1152); and

setting an indicator (it is taught as update state of the memory lines in the directory) to indicate that the data copied into the data processing system is valid.

Regarding claims 11 and 30, Gharachorloo teaches that further comprising: responsive to the accessing being a write access (Fig.12A, step 1200, col.13, section 0165, lines 3-5), obtaining identification of all nodes having containing the data to form a set of identified nodes (Col.5, section 0066, last six lines and Fig.12B, step 1230); and setting indicators in the set of identified nodes to indicate that the data is invalid in the set of identified nodes (Fig.12C, step 133).

Regarding claims 12 and 31, Gharachorloo teaches that the set of nodes is a set of data processing systems (Fig.1 and 2, sets of nodes 102 and 104 is a set of multiprocessor systems).

Regarding claims 13 and 32, Gharachorloo teaches that the data processing system includes a plurality of processors (col.3, section 0047) and wherein the method is a set of instructions executed by one of the plurality of processors (col.12, section 0153).

Regarding claims 14 and 33, Gharachorloo teaches that the data is a page (col.5, section 0064, lines 8-13).

Regarding claims 15 and 34, Gharachorloo teaches that the operation is read operation (Fig. 11A to 11E).

Regarding claims 16 and 35, Gharachorloo teaches that the operation is a write operation (Fig.12A to C).

Regarding claim 17, Gharachorloo teaches that a data processing system comprising: a bus system (Fig.1, intra-chip switch); a communications unit (Fig.1, output queue, router and input queue) connected to the bus system; a memory (memory subsystem 123) connected to the bus system, wherein the memory includes a set of

instructions (col.12, section 0153); and a processing unit (Fig.1, one of CPUs 106) connected to the bus system, wherein the processing unit executes the set of instructions to, place an indication (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) on a directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) identifying the data processing system as containing a copy of a data block with a location (state bits 2b in the directory entry 182) in the data processing system in which a flag (state field 186) associated the data block is located (col.12, section 0154) in response to initiating a read operation on the block of data(Fig.11A, step 1100, col.12, section 0154, lines 2-5); and send a message (it is taught as send read-exclusive request to the home node, Fig.12A, step 1214 to step 1230) to all other data processing systems identified in the directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) as containing a copy of the data block (Fig.12B, a shared copy of the memory line 184) to reset the flag (Fig.12B and Fig.12C, step 1203-1234) such that the flag indicates that the data in the data block is invalid (Fig.12C, step 1233-1234) without requiring any action by the other data processing systems receiving the message (col.14, section 0169, last 8 lines) in response to initiating a write operation on the data block (Fig.12A, step 1200, col.13, section 0165, lines 3-5).

Regarding claim 18, Gharachorloo teaches that a data processing system comprising: a bus system (Fig.1, intra-chip switch); a communications unit (Fig.1, output queue, router and input queue) connected to the bus system; a memory (memory

subsystem 123) connected to the bus system, wherein the memory includes a set of instructions (col.12, section 0153); and a processing unit (Fig.1, one of CPUs 106) connected to the bus system, wherein the processing unit executes the set of instructions to dedicate a processor within the plurality of processors for polling for request messages from other data processing systems (col.12, section 0153, lines 11-12); responsive to initiating a read operation to read data on a data block (Fig.11A, step 1100, col.12, section 0154, lines 2-5), posting an indication (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) on a directory of data blocks (it is taught as cache state directory 180 as shown in Fig.4) identifying the read operation by the data processing system (Fig.11A to Fig.11E); and responsive to initiating a write operation on the data block (Fig.12A, step 1200, col.13, section 0165, lines 3-5), sending a message (it is taught as send read-exclusive request to the home node, Fig.12A, step 1214 to step 1230) to all of the other data processing systems that the data block is invalid (Fig.12C, step 1233-1234) to remove the data block from the directory of data blocks (Fig.12C, step 1235; col.14, section 0167, last seven lines).

Regarding claim 19, Gharachorloo teaches that a data processing system comprising: a bus system (Fig.1, intra-chip switch); a communications unit (Fig.1, output queue, router and input queue) connected to the bus system; a memory (memory subsystem 123) connected to the bus system, wherein the memory includes a set of instructions (col.12, section 0153); and a processing unit (Fig.1, one of CPUs 106) connected to the bus system, wherein the processing unit executes the set of

instructions to identifying an operation to access the data (Fig. 11A, identifying a read operation for a memory line of information 184);

determining whether a copy of the data is present locally within the data processing system (Fig.11A, step 1102; col.12, section 0154, lines 5-6);

responsive to the copy of the data being present locally within the data processing system (Fgi.11A, step 1104), checking an indicator (check directory 180) for the data to determine whether the copy of the data is valid (check directory 180 to determine if the state of the memory line of information is exclusive which indicating a node has an exclusive copy of the corresponding memory line of information); and

responsive to the data being valid, accessing the copy of the data (Fig.11b, step 1158).

Regarding claim 37, Gharachorloo teaches that a computer program product in a computer readable medium for managing a plurality of caches of data, wherein the data processing system includes a plurality of processors (Fig.1 and 2, CPUs 106), the computer program product comprising:

first instructions for dedicating a processor within the plurality of processors for polling for request messages from other data processing systems (col.12, section 0153, lines 11-12);

second instructions, responsive to initiating a read operation to read data on a data block (Fig.11A, step 1100, col.12, section 0154, lines 2-5), for posting an indication (Fig.4, directory state such as invalid, exclusive, shared and shared-cv) on a directory of

data blocks (it is taught as cache state directory 180 as shown in Fig.4) identifying the read operation by the data processing system (Fig.11A to Fig.11E); and

third instructions, responsive to initiating a write operation on the data block (Fig.12A, step 1200, col.13, section 0165, lines 3-5), for sending a message (it is taught as send read-exclusive request to the home node, Fig.12A, step 1214 to step 1230) to all of the other data processing systems that the data block is invalid (Fig.12C, step 1233-1234) to remove the data block from the directory of data blocks (Fig.12C, step 1235; col.14, section 0167, last seven lines).

Regarding claim 38, Gharachorloo teaches that a computer program product in a computer readable medium for managing data in a distributed buffer system,

the computer program product comprising: first instructions for identifying an operation to access the data (col.12, section 0153, it is taught as a SEND instruction);

second instructions for determining whether a copy of the data is present locally within the data processing system (col.12, section 0153, it is taught as a RECEIVE instruction; section 0154, lines 5-6);

third instructions, responsive to the copy of the data being present locally within the data processing system, for checking an indicator for the data to determine whether the copy of the data is valid (col.12, section 0153, it is taught as a TEST instruction; section 0154, lines 6-8); and

fourth instructions, responsive to the data being valid, for accessing the copy of the data (col.12, section 0153, it is taught as a LSEND instruction).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Beardsley et al	US 6438661 B1
Michael et al	US 2001/0010068 A1
Wilson et al	US 6560681 B1
Ito et al	US 6654769 B2
Schoinas	US 6662276 B2
Masri et al	Us 2002/0078304 A1
Chilton	US 2002/0078292 A1
Khare et al	US 2002/0078305 A1

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song
Patent Examiner
March 17, 2004

Mano Padmanabhan
3/19/04
Supervisory Patent Examiner
Technology Center 2100